Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

1. (currently amended) An editing system for moving images, the editing system comprising:

a frame-random access store for storing image data representing a sequence of image frames which together form a moving image, the store storing data in an input format as captured such that the frames can be accessed in a random order;

an input circuit for receiving from a source data representing sequences of image frames in a plurality of input formats, wherein each of said sequences of image frames are captured at a first frame rate, the data representing each frame in a sequence as a first multiplicity of image lines which together form the image frame, and wherein each of said input format is defined by said first frame rate and said first multiplicity of [[data]] image lines, and for transferring the image data in said input formats to the frame-random access store;

wherein said store is adapted to store said image data in said plurality of input formats;

an editing processor for editing data read from the store at a processed data rate to produce data representing an edited sequence of image frames; and

an output circuit for outputting edited data from said store in a plurality of output formats,

wherein each of said edited data represent an edited sequence of image frames at a second frame rate, the data being output at an output data rate and representing each frame in the edited sequence as a second multiplicity of image lines which together form the image frame,

wherein each of said output formats is defined by said second frame rate and said second

multiplicity of [[data]] image lines,

and wherein the respective input and output format for data representing a sequence of image data are either the same or different.

2. (previously presented) An editing system for moving images, the editing system comprising:

a frame-random access store for storing image data representing a sequence of image frames which together form a moving image, the store storing data such that the frames can be accessed in a random order;

an input circuit for receiving from a source data representing one or more sequences of image frames captured at a first frame rate, the data being received at an input data rate and representing each frame in a sequence as a first multiplicity of image lines which together form the image frame, and for transferring the data to the frame-random access store;

an editing processor for editing data read from the store at a processed data rate to produce data representing an edited sequence of image frames;

an output circuit for outputting edited data representing an edited sequence of image frames at a second frame rate, the data being output at an output data rate and representing each frame in the edited sequence as a second multiplicity of image lines which together form the image frame; and

an asynchronous bus connecting said store, said input circuit, said editing processor and said output circuit, and wherein:

the input circuit comprises a decoder arranged to receive data synchronously from a source and a buffer for transferring data from the decoder to the asynchronous bus; and

the output circuit comprises an encoder arranged to output data synchronously to a destination and a buffer for transferring data from the asynchronous bus to the encoder.

3. (previously presented) An editing system as claimed in claim 2, further comprising a sizing circuit for varying the number of lines between said first multiplicity and said second multiplicity in each frame as data is transferred to the output circuit.

4. (previously presented) An editing system as claimed in claim 3, further comprising a monitor connected to receive data from the output circuit at said output data rate for display of said edited sequence thereon.

5. (previously presented) An editing system as claimed in claim 4, further comprising a linear store connected to receive data from the output circuit at said output data rate for storage of said edited sequence therein.

6. (previously presented) An editing system as claimed in claim 5, wherein said linear store comprises a video tape recorder selectively operable to output stored data at either said first frame rate or said second frame rate.

7. (previously presented) An editing system as claimed in claim 6, further comprising:

a user operable input device; and wherein the editing processor is connected to the frame-random access store and for processing data representing one or more image frames of one or more initial sequences in response to the user operable input device to produce processed data

representing an processed, edited sequence, which processed data is stored in the frame-random access store.

8. (previously presented) An editing system as claimed in claim 7, wherein said one or more initial sequences are captured at a frame rate of 24 per second and each frame comprises 625 image lines, and the input circuit is arranged to receive the data and transfer the same to the store at an input rate substantially corresponding to 25 frames per second and 625 lines.

9. (previously presented) An editing system as claimed in claim 8, wherein said processor is arranged to edit data at a processed data rate substantially corresponding to 24 frames per second and 625 lines, and the output circuit is arranged to output data at an output data rate substantially corresponding to the processed data rate.

10. (previously presented) An editing system as claimed in claim 8, wherein said processor is arranged to edit data at a processed data rate substantially corresponding to 24 frames per second and 625 lines, and the output circuit is arranged to output data at an output data rate substantially corresponding to 30 frames per second and 525 line.

11. (previously presented) An editing system as claimed in claim 10, wherein said processor is arranged to extract frame data from the frame-random access store as pairs of interleaved fields and to repeat the transfer of one field of each pair to the output circuit thereby causing the output circuit to output the edited sequence at said frame rate of 30 per second.

12. (previously presented) An editing system as claimed in claim 11, wherein said edited sequence comprises image frames derived from a first initial sequence comprising frames at a first frame rate and first line rate and image frames derived from a second initial sequence comprising frames at a second frame rate and second line rate different than said first frame and line rates, and wherein said processor is arranged to process the data for each frame in the edited sequence to conform to a line and frame rate corresponding to said output data rate.

Claims 13-14 (canceled).

15. (previously presented) An editing system as claimed in claim 1, further comprising a sizing circuit for varying the number of lines between said first multiplicity and said second multiplicity in each frame as data is transferred to the output circuit.

16. (previously presented) An editing system as claimed in claim 15, further comprising a monitor connected to receive data from the output circuit at said output data rate for display of said edited sequence thereon.

17. (previously presented) An editing system as claimed in claim 16, further comprising a linear store connected to receive data from the output circuit at said output data rate for storage of said edited sequence therein.

18. (previously presented) An editing system as claimed in claim 17, wherein said linear store comprises a video tape recorder selectively operable to output stored data at either said first

frame rate or said second frame rate.

19. (previously presented) An editing system as claimed in claim 18, further comprising:

a user operable input device; and wherein the editing processor is connected to the frame-random access store and for processing data representing one or more image frames of one or more initial sequences in response to the user operable input device to produce processed data representing an processed, edited sequence, which processed data is stored in the frame-random access store.

20. (previously presented) An editing system as claimed in claim 19, wherein said one or more initial sequences are captured at a frame rate of 24 per second and each frame comprises 625 image lines, and the input circuit is arranged to receive the data and transfer the same to the store at an input rate substantially corresponding to 25 frames per second and 625 lines.

21. (previously presented) An editing system as claimed in claim 15, further comprising a linear store connected to receive data from the output circuit at said output data rate for storage of said edited sequence therein.

22. (previously presented) An editing system as claimed in claim 21, wherein said linear store comprises a video tape recorder selectively operable to output stored data at either said first frame rate or said second frame rate.

23. (previously presented) An editing system as claimed in claim 22, further comprising:

a user operable input device; and wherein the editing processor is connected to the frame-random access store and for processing data representing one or more image frames of one or more initial sequences in response to the user operable input device to produce processed data representing an processed, edited sequence, which processed data is stored in the frame-random access store.

24. (previously presented) An editing system as claimed in claim 23, wherein said one or more initial sequences are captured at a frame rate of 24 per second and each frame comprises 625 image lines, and the input circuit is arranged to receive the data and transfer the same to the store at an input rate substantially corresponding to 25 frames per second and 625 lines.

25. (previously presented) An editing system as claimed in claim 1, further comprising a monitor connected to receive data from the output circuit at said output data rate for display of said edited sequence thereon.

26. (previously presented) An editing system as claimed in claim 1, further comprising a linear store connected to receive data from the output circuit at said output data rate for storage of said edited sequence therein.

27. (previously presented) An editing system as claimed in claim 26, wherein said linear store comprises a video tape recorder selectively operable to output stored data at either said first frame rate or said second frame rate.

28. (previously presented) An editing system as claimed in claim 27, further comprising:

a user operable input device; and wherein the editing processor is connected to the frame-random access store and for processing data representing one or more image frames of one or more initial sequences in response to the user operable input device to produce processed data representing an processed, edited sequence, which processed data is stored in the frame-random access store.

29. (previously presented) An editing system as claimed in claim 28, wherein said one or more initial sequences are captured at a frame rate of 24 per second and each frame comprises 625 image lines, and the input circuit is arranged to receive the data and transfer the same to the store at an input rate substantially corresponding to 25 frames per second and 625 lines.

30. (previously presented) An editing system as claimed in claim 1, further comprising:

a user operable input device; and wherein the editing processor is connected to the frame-random access store and for processing data representing one or more image frames of one or more initial sequences in response to the user operable input device to produce processed data representing an processed, edited sequence, which processed data is stored in the frame-random access store.

31. (previously presented) An editing system as claimed in claim 30, wherein said one or more initial sequences are captured at a frame rate of 24 per second and each frame comprises 625 image lines, and the input circuit is arranged to receive the data and transfer the same to the store at an input rate substantially corresponding to 25 frames per second and 625 lines.

32. (previously presented) An editing system as claimed in claim 2, further comprising a monitor connected to receive data from the output circuit at said output data rate for display of said edited sequence thereon.

33. (previously presented) An editing system as claimed in claim 2, further comprising a linear store connected to receive data from the output circuit at said output data rate for storage of said edited sequence therein.

34. (previously presented) An editing system as claimed in claim 33, wherein said linear store comprises a video tape recorder selectively operable to output stored data at either said first frame rate or said second frame rate.

35. (previously presented) An editing system as claimed in claim 34, further comprising:

a user operable input device; and wherein the editing processor is connected to the frame-random access store and for processing data representing one or more image frames of one or more initial sequences in response to the user operable input device to produce processed data representing an processed, edited sequence, which processed data is stored in the frame-random access store.

36. (previously presented) An editing system as claimed in claim 35, wherein said one or more initial sequences are captured at a frame rate of 24 per second and each frame comprises 625 image lines, and the input circuit is arranged to receive the data and transfer the same to the

store at an input rate substantially corresponding to 25 frames per second and 625 lines.

37. (previously presented) An editing system as claimed in claim 1, wherein said one or more initial sequences are captured at a frame rate of 24 per second and each frame comprises 625 image lines, and the input circuit is arranged to receive the data and transfer the same to the store at an input rate substantially corresponding to 25 frames per second and 625 lines.

38. (previously presented) An editing system as claimed in claim 37, wherein said processor is arranged to edit data at a processed data rate substantially corresponding to 24 frames per second and 625 lines, and the output circuit is arranged to output data at an output data rate substantially corresponding to the processed data rate.

39. (previously presented) An editing system as claimed in claim 37, wherein said processor is arranged to edit data at a processed data rate substantially corresponding to 24 frames per second and 625 lines, and the output circuit is arranged to output data at an output data rate substantially corresponding to 30 frames per second and 525 line.

40. (previously presented) An editing system as claimed in claim 39, wherein said processor is arranged to extract frame data from the frame-random access store as pairs of interleaved fields and to repeat the transfer of one field of each pair to the output circuit thereby causing the output circuit to output the edited sequence at said frame rate of 30 per second.